29.4 A 237mW aDSL2+ CO Line Driver in Standard 1.2V 0.13µm CMOS

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The persistent growing demand for broadband internet has triggered the telephone companies to improve the xDSL standards to bridge the last mile between the central office (CO) and the end user. The aDSL2+ standard doubles the bandwidth of an aDSL system to 2.2MHz and hence increases the bit rate up to 24Mb/s. The high crest factor (CF) of discrete multi-tone (DMT) modulated signals poses serious problems for an efficient and low-cost implementation of the line driver [1]. In the nano-electronic era, the line driver remains more than ever the major bottleneck for lowering the cost and power. The low supply voltages coming from nanometer technologies increase the current density in the line driver. Together with the high CF and the doubled bandwidth, a highly efficient aDSL2+ line driver in a low-voltage, low-cost CMOS technology seems to be a contradiction.

The aDSL2+ line driver presented here is a self oscillating power amplifier (SOPA) with a high-voltage output buffer in standard 1.2V 0.13µm CMOS. A SOPA line driver can be quite successful in sub-micrometer technologies, since it can drive DMT signals with a high CF efficiently [2]. But, as with any power amplifier, its efficiency and reliability drop with decreasing supply voltage. An aDSL2+ system delivers an average of 20dBm to a 100Ω twisted-pair line. Lowering the supply voltage thus results in an increased current density for a constant output power. This in turn increases hot carrier generation and electro-migration, both of which affect the reliability of the driver. The large current also results in a drop in efficiency because of the increased switching and conduction losses of the driver. Moreover, the large CF causes the driver to put signals with a high voltage-swing on the line. Since the output voltage-swing of the driver is limited by its supply voltage, a transformer with a high turns-ratio has to be used. The large return signal attenuation then limits the practical use of the line driver.

To overcome these low-voltage issues, a high-voltage output buffer is included in the SOPA architecture. The high-voltage buffer is, like all the building blocks in this line driver, designed in a standard, submicron CMOS technology. Therefore, it is demonstrated that the use of extra mask sets to create high-voltage devices, such as LDMOS or thick-oxide transistors, can be avoided. This simplicity makes this line driver very attractive in terms of cost and the prospects for integration.

Figure 29.4.1 shows the block diagram of the line driver. The single SOPA comprises a continuous-time RC integrator followed by a non-clocked comparator. The SOPA is thus an asynchronous switching-type amplifier. The high-voltage buffer converts the output of the comparator to high voltage levels. The output of this buffer is fed back to the integrator using a loop filter. Since the integrator and comparator operate at the low, nominal supply voltage of the technology, the output of this buffer needs to be down converted within the voltage limits of the technology. This down conversion is implemented in two stages. The 1st stage implements a voltage division set by resistors R_3 and R_4 in the loop filter. The 2nd implements a current division set by resistors R_1 and R_2 at the input of the integrator. The advantage of an RC integrator is its high linearity for large input signals since the input node can be considered as a virtual ground.

The frequency of the self-oscillation is set by the loop filter in combination with the filter in the forward path. The self-oscillation provides a dithering effect for the input signal and hence linearizes the comparator for frequencies lower than the self-oscillation frequency. The addition of the integrator introduces noise shaping into the SOPA system, which decreases the distortion of the signal at the output since higher frequencies are attenuated more in the loop. Two single SOPA's are connected in a bridge configuration, which ensures the necessary output voltage swing and a galvanic decoupling towards the line. Because of the asynchronous behavior of the two SOPA's, their self-oscillation frequencies tend to get pulled towards each other [2]. This provides extra filtering since the oscillation frequency becomes a common-mode signal and is, as such, not transferred to the load.

Figure 29.4.2 shows the block schematic of the high-voltage buffer. The output stage is composed of 5 stacked transistors for the pull-up circuit and another 5 for the pull-down circuit. Given the switching behavior of the driver, the stacked transistors are driven by a dedicated bias circuit to keep the voltage across their terminals within the technology limit, the nominal supply voltage V_{DD}. The theoretical maximum supply voltage for the buffer is thus 5 times V_{DD}. The output of the buffer is controlled by the outer stacked transistors, which are driven by a tapered buffer. Distortion of the output waveform is minimized by providing matched delay paths from the output of the comparator to the outer stacked transistors. This approach uses a symmetrical supply with two level-shift circuits for setting the offset voltages of the pMOS and nMOS buffers. The level shifters are preceded by a non-overlapping switching circuit, since short-circuit currents in the output stage can lead to significant power dissipation at high voltages.

Figure 29.4.3 depicts the bias circuit implementation for the stacked transistors based on the techniques used in [3]. The bias voltages are set by a resistive ladder network implemented with standard CMOS transistors. The capacitors limit the transient voltage peaks caused by the large gate-drain capacitances of the stacked transistors during switching. Optimization of the transistor widths and the capacitor values leads to high-speed, reliable operation of the high-voltage buffer.

The chip has been processed in a mainstream 1.2V 0.13µm triple-well 1P6M CMOS technology. The triple-well process permits a source-bulk connection without substrate losses. The integrator and comparator operate at the nominal supply voltage of 1.2V, whereas the high-voltage buffer operates at 5.5V. This is more than 4.5 times the nominal supply with only 5 stacked transistors. Figure 29.4.4 shows the measured self-oscillation frequency of a single SOPA. The self-oscillation frequency of 25MHz is set by the filters and an output voltage swing of 4.7V is achieved with a load of 12.5Ω. A DMT signal consisting of 512 tones with a tone-spacing of 4.3125kHz is applied to the driver to derive the missing tone power ratio (MTPR). Tones 1 to 64 are left unused to form the upstream tones and tones 102, 183, 286, 381 and 462 are left out as antenna tones. Figure 29.4.5 shows an MTPR measurement of the antenna tone at the highest and most critical frequency. An MTPR of 58dB has been achieved for a DMT signal with an average output power of 20dBm and a CF of 5.6. The total power dissipation is 237mW resulting in an efficiency of 42%. Figure 29.4.6 summarizes the process and performance specifications. A die micrograph of the aDSL2+ line driver is shown in Fig. 29.4.7. The die occupies an area of 4.1mm×2.0mm.

References:

[1] L. Cloetens, "Broadband Access: The Last Mile," *ISSCC Dig. Tech. Papers*, pp. 18-21, 2001.

[2] T. Piessens and M. Steyaert, "SOPA: A High Efficiency Line Driver in 0.35µm CMOS using a Self-Oscillating Power Amplifier," *ISSCC Dig. Tech. Papers*, pp. 306-307, 2001.

[3] B. Serneels, M. Steyaert and W. Dehaene, "A 5.5 V SOPA Line Driver in a Standard 1.2 V 0.13µm CMOS Technology," *Proc. ESSCIRC*, pp. 303-306, 2005.

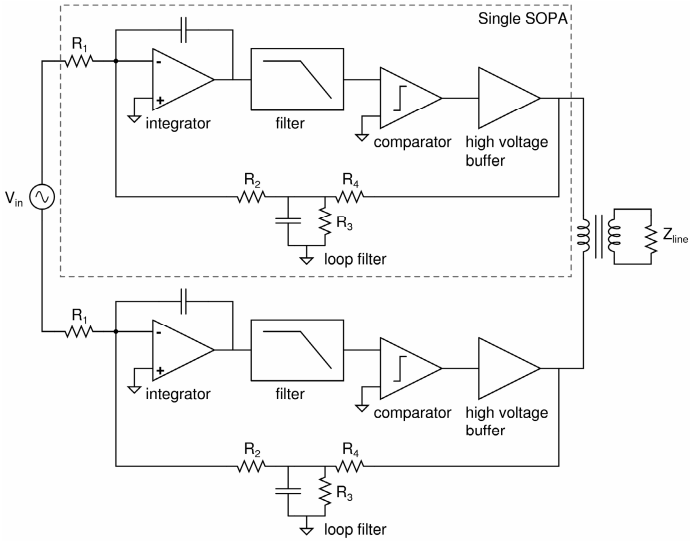

Figure 29.4.1: Block diagram of the line driver.

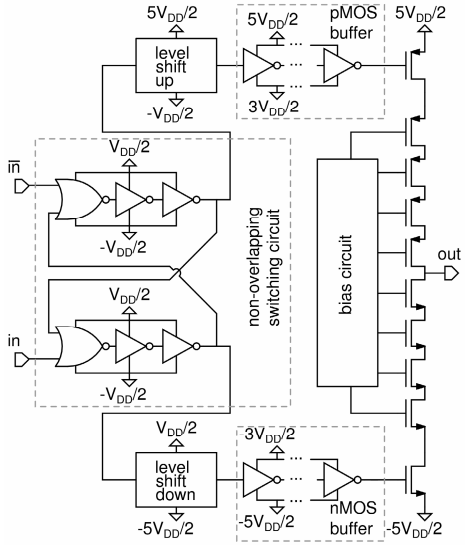

Figure 29.4.2: Block schematic of the high-voltage buffer with symmetrical supplies.

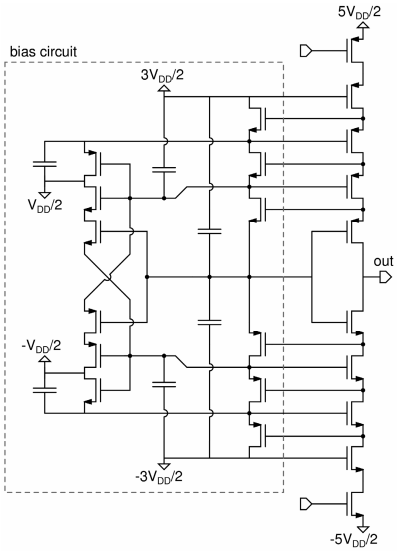

Figure 29.4.3: Bias circuit implementation for the stacked transistors.

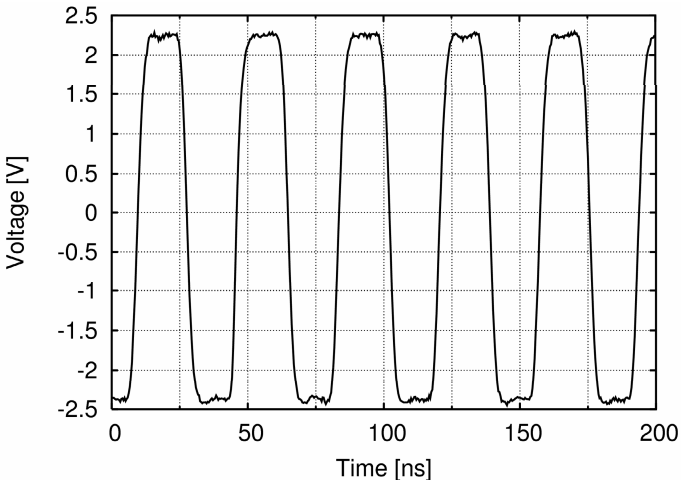

Figure 29.4.4: Measured output square wave of a single SOPA at the input of the transformer, showing the self-oscillation frequency of 25MHz with an output voltage swing of 4.7V.

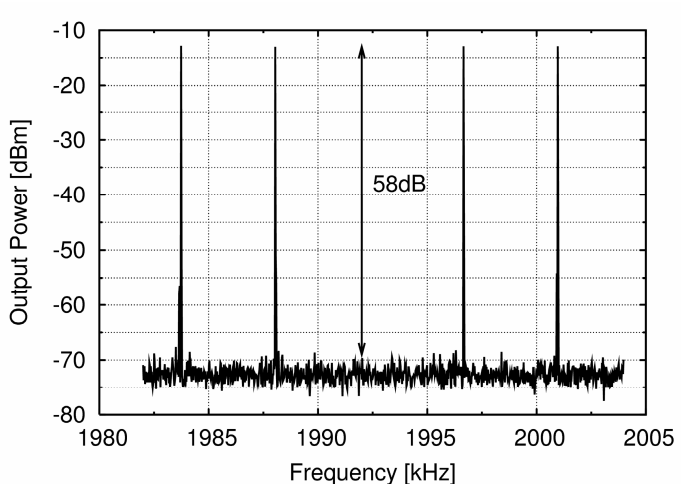

Figure 29.4.5: A 58dB MTPR line measurement around tone 462.

Parameter	This work	aDSL2+ specification
Technology	130nm CMOS 1P6M	
Nominal Supply Voltage	1.2V	
High Supply Voltage	5.5V	
Ouput Voltage Swing @12.5Ω	4.7V	
Bandwidth	>2.2MHz	2.2MHz
Output Power	20dBm	20dBm
Crest Factor	5.6	>5
MTPR	58dB	55dB
Total Power Consumption	237mW	
Efficiency	42%	

Figure 29.4.6: Measured line performance summary.

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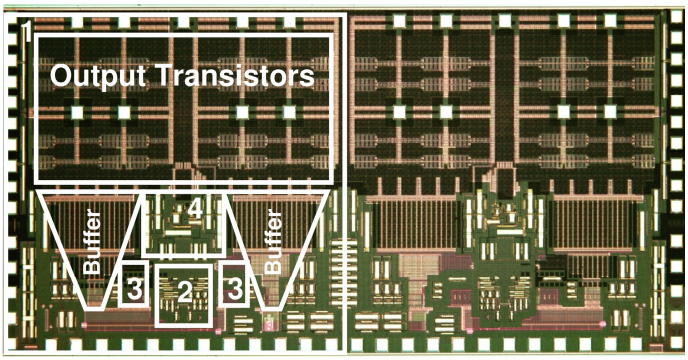

1. Single SOPA
2. Integrator and comparator
3. Level shifter
4. Bias circuit

Figure 29.4.7: Die micrograph of the a DSL2+ CO line driver.

